## SUBMISSION OF REPLACEMENT FORMAL DRAWINGS

Submitted herewith is a replacement drawing sheet for Figures 8A-8E and a replacement drawing sheet for Figures 10A-10D.

Approval and entry of these replacement drawing sheets are respectfully requested.

## REMARKS

In view of the above amendments and following remarks, reconsideration of the rejections and further examination are requested.

Claims 1-6 are pending in this application. Claims 1-6 have been rejected. Claim 1-6 are amended herein. No new subject matter has been added.

The specification and abstract have been carefully reviewed and revised to make grammatical and idiomatic improvements in order to aid the Examiner for further consideration of the application. A substitute specification and abstract including the revisions have been prepared and are submitted herewith. No new matter has been added. Also submitted herewith are marked up copies of the substitute specification and abstract indicating the changes incorporated therein.

The drawings have been objected to. More specifically, the Examiner objected to the drawings because Figures 8(a), 8(b) and 8(c) are labeled pulse voltage for address "lectrodes". The Examiner suggested that "electrodes" is more appropriate. Figure 8 has been amended as suggested by the Examiner and to specifically identify each of the five figures contained therein as Figures 8A-8E. Moreover, the Applicants have amended Figure 10 to more specifically identify each of the four figures contained therein as figures 10A-10D. No new matter has been added by these revisions.

For at least the reasons set forth above, the Applicants respectfully request that the objection to the drawings be withdrawn.

Claims 1-4 and 6 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kato et al. (U.S. Patent No. 6,376,995) (hereinafter referred to as "Kato") in view of Kado et al. (U.S. Patent No. 6,666,738) (hereinafter referred to as "Kado") and further in view of Hirano et al. (U.S. Patent Application Publication No. 2003/0030377) (hereinafter referred to as "Hirano").

The above-mentioned rejections are submitted to be inapplicable to the amended claims for the following reasons.

Claim 1 is patentable over the combination of Kato, Kado and Hirano because claim 1 requires a method of manufacturing a plasma display panel including a scan electrode, a

sustained electrode, and an address electrode, including, in part, short circuiting the scan electrode, the sustained electrode, and the address electrode. Moreover, claim 1 requires alternately applying a scan electrode pulse voltage and a sustained electrode pulse voltage at least across the scan electrode and the sustain electrode, wherein the first pulse voltage has a first pulse voltage rising edge timing synchronized with a scan electrode pulse voltage rising edge timing and a pulse width smaller than a width of the scan electrode pulse voltage, and the second pulse voltage has a second pulse voltage rising edge timing synchronized with a sustain electrode pulse voltage rising edge timing and a pulse width smaller than a width of the sustain electrode pulse voltage.

In contrast, Kato discloses a plasma display panel having ribs 26 disposed in such a manner that they form stripes. Two address electrodes 23 are disposed in each emission unit parallel to the ribs 26. A pair of first and second electrodes 21 and 22, respectively, form a scan electrode and a sustain electrode, and are disposed transversely and perpendicularly to the address electrodes 23. The electrodes 21 and 22 are covered with a transparent dielectric layer 24 and a protective layer 25. The two electrodes 23 disposed in the emission unit are electrically connected to each other. It should be understood that the scan electrodes 21, the sustain electrodes 22, and the address electrodes 23 are controlled independently. Notably, Kato does not disclose short-circuiting the scan electrodes 21, the sustain electrodes 22 and the address electrodes 23 during the aging process.

Figure 51 of Kato shows waveforms of the applied pulses used to drive the plasma display device. The applied pulses are composed of four stages: the set-up period; the address period; the sustain period; and the erase period.

The sustain period shows sustain pulses that start from the electrode 21. Thus, positive charge is needed on the electrodes 21 and negative charge is needed on the electrodes 22 and 23. This charge is accumulated in the pixels where the address discharge was generated in the second stage. The initial sustain pulses are applied only on the electrode 21. Discharge occurs between the electrodes 22 and 21 as is the case with the conventional method. However, the following sustain pulses are applied on the electrodes 23 and 22, leading to discharge between the

electrodes 22 and 21 as well as the electrodes 23 and 21. Notably, as shown in the sustain period of Figure 51, the rising time of the address electrode pulses is not synchronized to coincide with the rising time of the sustain electrode pulses or the scan electrode pulses.

Based on the above discussions, it is apparent that the method of driving a plasma display device of Kato controls the scan electrodes 21, the sustain electrodes 22 and the address electrodes 23, independently, rather than short-circuiting them during an aging process. Kato also uses address electrode pulses that are not synchronized to coincide with the rising time of the sustain electrode pulses or the scan electrode pulses. Moreover, there is no disclosure or suggestion in Kato to short-circuit the scan 21, sustain 22 and address 23 electrodes, or to apply the address electrode 23 pulses such that they coincide, or are synchronized with, the rising time of the sustain 22 or scan electrode 21 pulses. In other words, the apparatus and method of Kato does not describe a method of manufacturing a plasma display panel including a scan electrode, a sustain electrode, and an address electrode, including, in part, short circuiting the scan electrode, the sustain electrode, and the address electrode, and alternately applying a scan electrode pulse voltage and a sustain electrode pulse voltage at least across the scan electrode and the sustain electrode, wherein the first pulse voltage has a first pulse voltage rising edge timing synchronized with a scan electrode pulse voltage rising edge timing and a pulse width smaller than a width of the scan electrode pulse voltage, and a second pulse voltage has a second pulse voltage rising edge timing synchronized with a sustain electrode pulse voltage rising edge timing and a pulse width smaller than a width of the sustain electrode pulse voltage as recited in claim 1.

Regarding Kado, it is relied upon in rejection as disclosing that during a plasma display panel manufacturing process a plasma display panel must be aged in order to stabilize the luminescence and discharge characteristics of the display. More specifically, Kado discloses a method of manufacturing a plasma display panel that minimizes phosphor deterioration and that provides a comparatively high luminescence efficiency as well as high quality color reproduction.

An aging device 50 is provided for performing the aging process. The aging device 50 is constructed from pipes 52a and 52b, valves 53a and 53b and a driving circuit 54. The pipes 52a

and 52b circulate a discharge gas through the inside of a panel 51. The valves 53a and 53b regulate the pressure of the discharge gas inside the panel 51. The driving circuit 54 is used to apply a voltage as a pulse.

After a vacuum is formed inside the panel 51 using the pipe 52a, a discharge gas 58 is introduced using the pipe 52b. The valves 53a and 53b are then adjusted so that the discharge gas will then continue to flow at a certain flow rate while being maintained at a certain pressure.

After the gas pressure is regulated, a certain voltage is applied to the discharge electrodes formed in the front plate 58 using the driving circuit 54, while the gas is still circulating through the inside of the panel. This generates a discharge inside the panel 51, which is then aged for a certain time period. By continuing to produce a discharge while circulating the discharge gas inside the panel 51, gas, including steam generated inside the panel, can be evacuated, and the deterioration in the luminescence characteristics of the phosphor layer generated during aging is reduced. Kado does not disclose using address electrodes. However, as with Kato, it is clear that Kado also fails to disclose or suggest the above-discussed short circuiting and synchronization features of the claimed method of manufacturing a plasma display panel as recited in claim 1. Therefore, Kado fails to address the deficiencies of Kato.

As for Hirano, it is relied upon as disclosing that aging of the plasma display panel is done by driving the plasma display panel under practical conditions. Specifically, Hirano discloses aging a plasma display panel in a constant cycle from sustaining discharge through priming to write discharge. That is, under practical use of a plasma display panel. However, Hirano also fails to disclose or suggest the above-discussed short circuiting and synchronization features of the claimed method of manufacturing a plasma display panel as recited in claim 1.

Regarding claim 6, it is patentable over the references relied upon in the rejection for reasons similar to those set forth above in support of claim 1. That is, claim 6 recites a method of manufacturing a plasma display panel including a scan electrode, a sustain electrode, and an address electrode, including, in part, short circuiting the scan electrode, the sustain electrode, and the address electrode, which features are not disclosed or suggested by the references.

Accordingly, no obvious combination of the teachings of Kato, Kado and Hirano, would result in, or otherwise render obvious, the invention recited in claims 1-4 and 6.

Claim 5 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kato in view of Kado and Hirano, and further in view of Chung (U.S. Patent Application Publication No. 2003/0141815).

Kato, Kado and Hirano are discussed above. Regarding Chung, it is relied upon in the rejection as disclosing applying lower discharge voltages during aging to examine the plasma display panel as time increases. Specifically, Chung discloses a process of removing impurities of upper and lower substrates 36, 38 by using at least one of a plasma-cleaning process or a heating process.

However, it is clear that Chung also fails to disclose or suggest the above-discussed short circuiting and synchronization features of the claimed method of manufacturing a plasma display panel as recited in claim 1. Therefore, Chung fails to address the deficiencies of Kato, Kado and Hirano. Accordingly, no obvious combination of the teachings of Kato, Kado, Hirano and Chung would result in, or otherwise render obvious, the invention recited in claim 5.

Because of the above-mentioned distinctions, it is believed clear that claims 1-6 are patentable over the references relied upon in the rejections. Therefore, it is submitted that claims 1-6 are clearly allowable over the prior art of record.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action are respectfully solicited.

Should the Examiner believe there are any remaining issues that must be resolved before this application can be passed to issue, it is respectfully requested that the Examiner contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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